Claims

1. A ballast, comprising:

an inverter, comprising:

first and second input terminals adapted to receive a source of substantially direct current (DC) voltage;

an inverter output terminal;

an output circuit coupled to the inverter output terminal, the output circuit comprising first and second output connections for coupling to a lamp load comprising at least one gas discharge lamp;

a fault detection circuit coupled between the output circuit and the inverter, wherein the fault detection circuit is operable:

(i) to monitor a first signal and a second signal within the output circuit;

(ii) to set a fault threshold in dependence on the second signal; and

(iii) in response to the first signal exceeding the fault threshold, to issue a shutdown command directing the inverter to cease operation.

2. The ballast of claim 1, wherein the second signal is indicative of the type of lamps in the lamp load.

3. The ballast of claim 1, wherein the fault threshold is set at:

(i) a first level in response to the second signal being less than a first predetermined value;

(ii) a second level that is greater than the first level in response to the second signal being greater than the first predetermined level but less than a second predetermined value; and

(iii) a third level that is greater than the second level in response to the second signal being greater than the second predetermined level.

4. The ballast of claim 3, wherein the second signal is:

(i) less than the first predetermined level when the lamp load consists of F17T8 lamps;

(ii) greater than the first predetermined level but less than the second predetermined level when the lamp load consists of F25T8 lamps; and

(iii) greater than the second predetermined level when the load consists of F32T8 lamps.

5. The ballast of claim 1, wherein the fault detection circuit comprises:

first and second inputs coupled to the output circuit; and

an output coupled to the inverter.

6. The ballast of claim 5, wherein:

the output circuit further comprises:

a resonant inductor coupled between the inverter output terminal and the first output connection; and

a resonant capacitor coupled between the first output connection and the second input of the fault detection circuit; and

the first input of the fault detection circuit is coupled to the first output connection of the output circuit.

7. The ballast of claim 6, wherein:

the first signal is indicative of the voltage across the resonant capacitor; and

the second signal is indicative of the current flowing through the resonant capacitor.

8. The ballast of claim 5, wherein:

the inverter further comprises:

upper and lower inverter transistors; and

an inverter driver circuit coupled to the upper and lower inverter transistors and operable to commutate the inverter transistors in a substantially complementary manner, the inverter driver circuit having a shutdown input, wherein the inverter driver circuit is operable, in response to receipt of the shutdown command at the shutdown input, to cease commutating the inverter transistors; and

the output of the fault detection circuit is coupled to the shutdown input of the inverter driver circuit.

9. The ballast of claim 8, wherein the inverter further comprises:

a current sensing resistor coupled in series with the lower inverter transistor; and

a diode having an anode coupled to the current sensing resistor and a cathode coupled to the shutdown input of the inverter driver circuit.

10. The ballast of claim 8, wherein the fault detection circuit further comprises:

a first diode having an anode coupled to circuit ground and a cathode coupled to the second input;

a second diode having an anode coupled to the second input and a cathode coupled to a first node;

a first resistor coupled between the first node and a second node;

a second resistor coupled between the second node and circuit ground;

a first transistor having a gate, a drain, and a source, the source being coupled to circuit ground;

a third resistor coupled between the second node and the gate of the first transistor;

a second transistor having a gate, a drain, and a source, the source being coupled to circuit ground;

a fourth resistor coupled between the first node and the gate of the second transistor;

a fifth resistor coupled between the first input and a third node;

a sixth resistor coupled between the third node and the drain of the first transistor;

a seventh resistor coupled between the drain of the first transistor and the drain of the second transistor;

an eighth resistor coupled between the drain of the second transistor and circuit ground;

a third transistor having a gate, a drain, and a source, the gate being coupled to the third node and the source being coupled to circuit ground;

a ninth resistor coupled between a direct current (DC) voltage supply and the drain of the third transistor;

a fourth transistor having a base, an emitter, and a collector, the base being coupled to the drain of the third transistor and the collector being coupled to the DC voltage supply;

a tenth resistor coupled between the emitter of the fourth transistor and circuit ground; and

a third diode having an anode coupled to the emitter of the fourth transistor and a cathode coupled to the output.

11. A ballast, comprising:

an inverter, comprising:

first and second input terminals adapted to receive a source of substantially direct current (DC) voltage;

an inverter output terminal;

upper and lower inverter transistors; and

an inverter driver circuit coupled to the upper and lower inverter transistors and operable to commutate the inverter transistors in a substantially complementary manner, the inverter driver circuit having a shutdown input, wherein the inverter driver circuit is operable, in response to receipt of a shutdown command at the shutdown input, to cease commutating the inverter transistors;

a fault detection circuit, comprising:

first and second inputs;

an output coupled to the shutdown input of the inverter driver circuit;

an output circuit, comprising:

first and second output connections for coupling to a lamp load comprising at least one gas discharge lamp;

a resonant inductor coupled between the inverter output terminal and the first output connection, the first output connection being coupled to the first input of the fault detection circuit; and

a resonant capacitor coupled between the first output connection and the second input of the fault detection circuit, the resonant capacitor having a resonant capacitor voltage and a resonant capacitor current; and

wherein the fault detection circuit is operable:

(i) to monitor the resonant capacitor voltage and the resonant capacitor current;

(ii) to set a fault threshold in dependence on the resonant capacitor current; and

(iii) in response to the resonant capacitor voltage exceeding the fault threshold, to send the shutdown command to the inverter driver circuit.

12. The ballast of claim 11, wherein the fault threshold is set at:

(i) a first level in response to the resonant capacitor current being less than a first predetermined value;

(ii) a second level that is greater than the first level in response to the resonant capacitor current being greater than the first predetermined level but less than a second predetermined value; and

(iii) a third level that is greater than the second level in response to the resonant capacitor current being greater than the second predetermined level.

13. The ballast of claim 12, wherein the resonant capacitor current is:

(i) less than the first predetermined level when the lamp load consists of F17T8 lamps;

(ii) greater than the first predetermined level but less than the second predetermined level when the lamp load consists of F25T8 lamps; and

(iii) greater than the second predetermined level when the load consists of F32T8 lamps.

14. The ballast of claim 11, wherein the inverter further comprises:

a current sensing resistor coupled in series with the lower inverter transistor; and

a diode having an anode coupled to the current sensing resistor and a cathode coupled to the shutdown input of the inverter driver circuit.

15. The ballast of claim 11, wherein the fault detection circuit further comprises:

a first diode having an anode coupled to circuit ground and a cathode coupled to the second input;

a second diode having an anode coupled to the second input and a cathode coupled to a first node;

a first resistor coupled between the first node and a second node;

a second resistor coupled between the second node and circuit ground;

a first transistor having a gate, a drain, and a source, the source being coupled to circuit ground;

a third resistor coupled between the second node and the gate of the first transistor;

a second transistor having a gate, a drain, and a source, the source being coupled to circuit ground;

a fourth resistor coupled between the first node and the gate of the second transistor;

a fifth resistor coupled between the first input and a third node;

a sixth resistor coupled between the third node and the drain of the first transistor;

a seventh resistor coupled between the drain of the first transistor and the drain of the second transistor;

an eighth resistor coupled between the drain of the second transistor and circuit ground;

a third transistor having a gate, a drain, and a source, the gate being coupled to the third node and the source being coupled to circuit ground;

a ninth resistor coupled between a direct current (DC) voltage supply and the drain of the third transistor;

a fourth transistor having a base, an emitter, and a collector, the base being coupled to the drain of the third transistor and the collector being coupled to the DC voltage supply;

a tenth resistor coupled between the emitter of the fourth transistor and circuit ground; and

a third diode having an anode coupled to the emitter of the fourth transistor and a cathode coupled to the output.

5